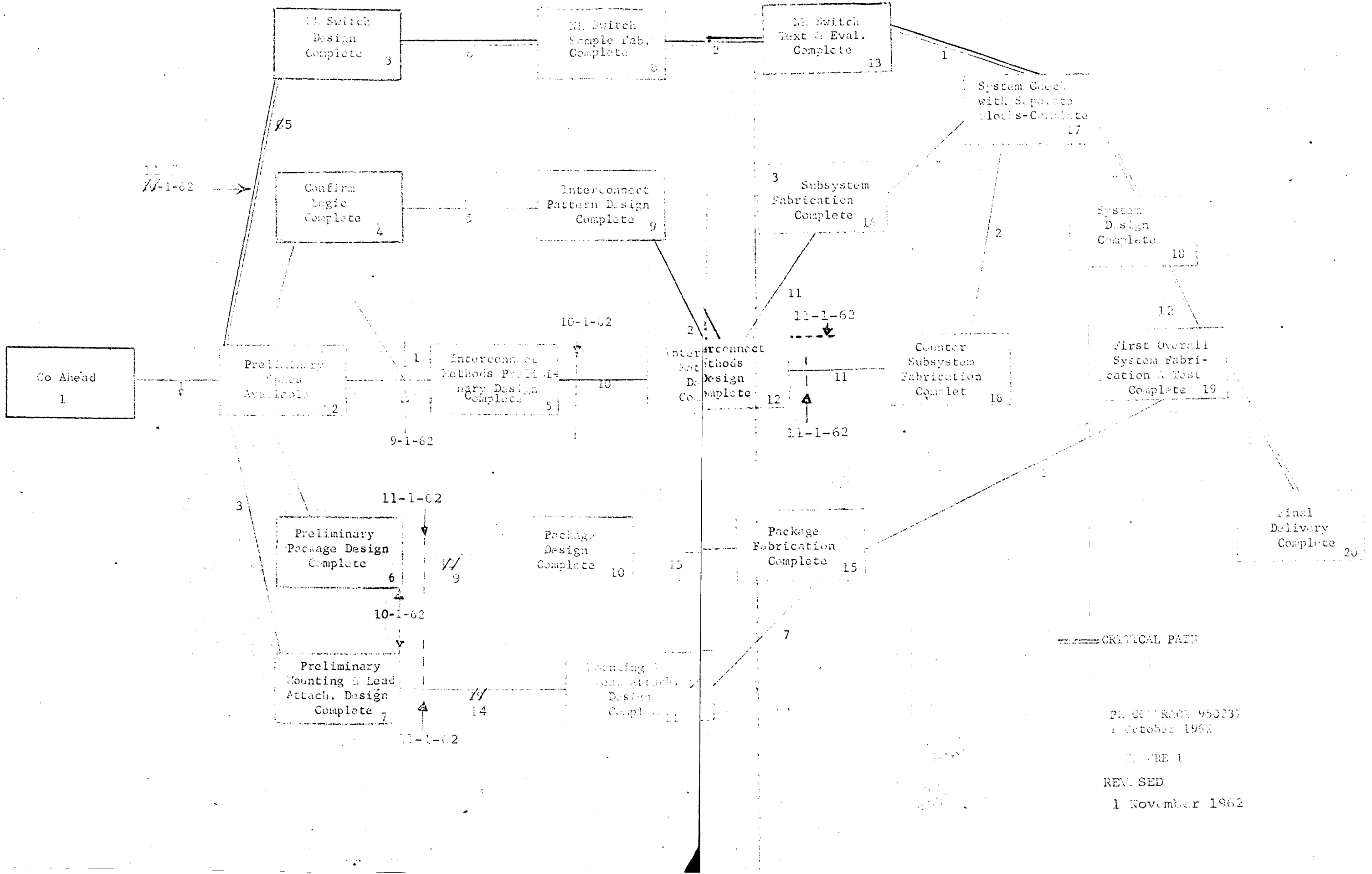
SECOND QUARTERLY REPORT
ON
MOLECULAR POWER SUPPLY
SYNCHRONIZER
FOR THE PERIOD
AUGUST THROUGH OCTOBER 31, 1962

JPL ORDER 950237
under
NAS 7-100

Westinghouse Electric Corporation
Astroelectronics Department
Newbury Park, California



PL SCHEDULE 950237
1 October 1962

FIGURE 1

REVISED

1 November 1962

LIST OF ILLUSTRATIONS

CONTRACT OBJECTIVES AND GENERAL APPROACH

The contract objectives have remained the same as those outlined in the first quarterly report, as has the general approach. However, development of devices and size reduction of devices has made possible a significant reduction in the size of the final block. We now anticipate that the logic portion of the block will measure .275 by .225 of an inch and that the over all combination of the logic and output switches will be a square .275"by .275". Details of the size reductions and the advantages gained by these reductions will be given under the appropriate headings.

PROJECT BREAKDOWN

Because there have been no changes in the objectives or general approach, the project breakdown shown in the first quarterly report has been maintained and progress within each of these sub-headings will be treated separately. Figure 1 is a PERT Diagram as of 1 November 1962. Figure 2 is a tabulation of path lengths from this PERT Diagram and shows that the longest path on this project has been reduced by some 5 weeks from that shown in the first quarterly report. This indication still shows a 5 week override from the target completion date, however, because of the tight control being maintained, it is hoped that this can be reduced to a point where delivery will be on schedule. The sub-projects will be treated in the following order:

(a) Logic design and confirmation.

(b) Interconnection pattern design.

(c) Interconnection method design and development.

(d) Output Switch (called non-linear load switch) electrical and device design.

(e) Packaging design.

(f) Partial systems fabrication.

(g) Overall system fabrication.

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TABULATION OF PERT CHART PATHS

1 NOVEMBER 1962

To 11-1-62	23	To 11-1-62	23	To 11-1-62	23	To 11-1-62	23	To 11-1-62	23
11-1-62 - 3	5	11-1-62 - 14	11	11-1-62-10	9	11-1-62-11	14	11-1-62-16	9
3 - 8	8	14 - 17	4	10 - 15	15	11 - 15	7	16 - 17	2
8 - 13	2	17 - 18	2	15 - 19	3	15 - 19	3	17 - 18	2
13 - 17	1	18 - 19	12	19 - 20	4	19 - 20	4	18 - 19	12
17 - 18	2	19 - 20	4					19 - 20	4
18 - 19	12								
19 - 20	4								
	57		56		54		51		52

Figure 2

LOGIC DESIGN

The logic design is now considered complete as indicated in the first quarterly report. Full logical operation was obtained with integrated circuitry elements and this item has now been delivered for evaluation. It has been under evaluation for a period of about six weeks and operation has been reported as satisfactory. The only item on this logic not covered in the first quarterly report was a test run to determine the sensitivity of this logic to rise time of the input signal. Because this is DC coupled type logic, it appeared theoretically possible to drive it even from a sine wave. This particular possibility was of interest in noise filtering for the input signal. Therefore, necessary tests were run and it was found that operation with a sine wave input was equally good with that of a square wave input, thus permitting filtering of the 38.4 KC input signal if this should be desired.

INTERCONNECT PATTERN DESIGN

During the current reporting period, the size and general geometry of the double NAND gates, which are a standard production item and from which this unit will be assembled, has been changed. This change has resulted in the possibility of forming this entire unit on a chip that measures .275 by .275 inches. The advantages of the reduced size, from a mounting point of view, are tremendous; however, becuase of the change in geometry our original interconnection pattern designs have become obsolete. The new geometry is shown in Figure 3 and it will be noted that as a part of this geometry the crossover interconnection tubs have been included as a part of the original masking. This permitted us to continue with a new interconnect pattern design based on this particular crossover tub placement. This design was at first concentrated into forming a binary counter because five such counters are required as a part of this project. The exact physical configuration for forming these counters in the final product was not made; instead, a binary pattern was designed for a block of four of these double NANDS because this block of four could readily be mounted on a standard TO-5 type header for test. The resulting pattern is shown in Figure 4. Designs for the overall logic with this new geometry are now in progress.

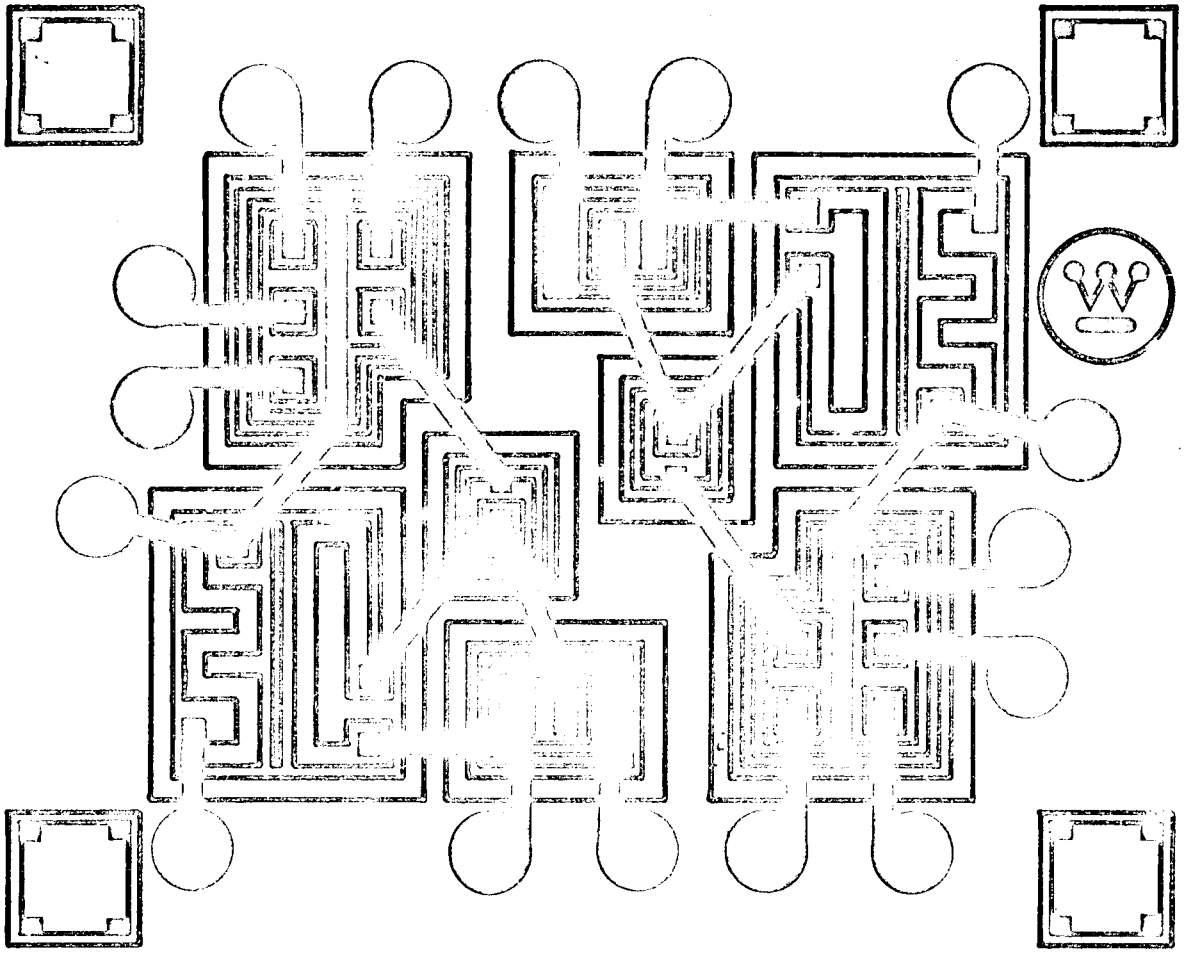

Figure 3

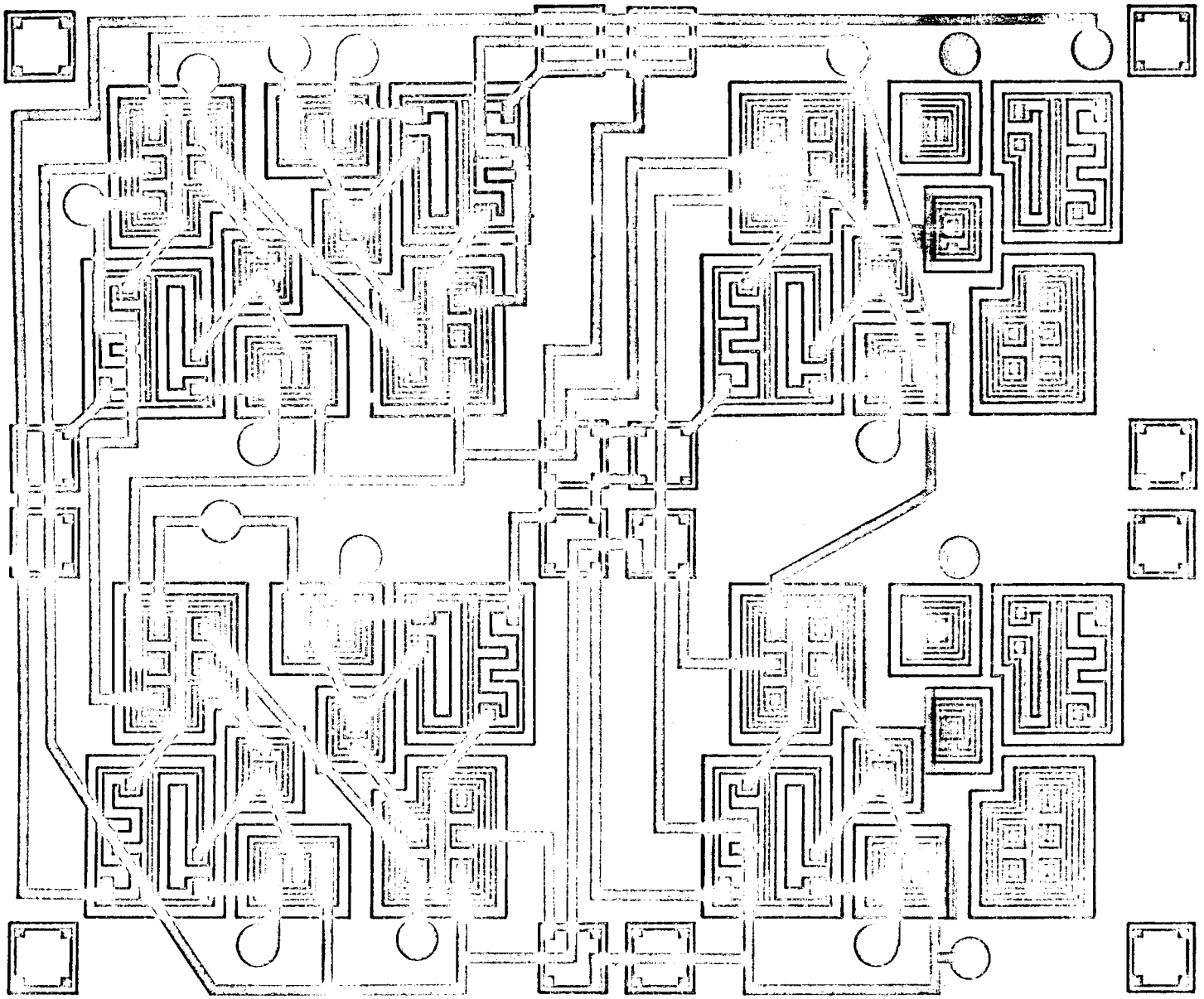

Figure 4

INTERCONNECTION METHOD DESIGN

Tests on the feasibility of using the substrate to carry the ground current were completed. A group of P type wafers with resistivity of .001 ohm centimeter and thickness of 4.5 mils was used to grow epitaxially a .2 ohm centimeter P film of about 22 microns. Point contact to back plane resistances of less than one ohm were obtained which indicated the impedance would be low enough to permit the required currents to flow. Effects of the multiple circuit use of this ground were not pursued at this time for reasons given below.

Further tests of the crossover method previously described were performed with favorable results. Values of resistance of less than 10 ohms were obtained.

In view of the favorable results, crossover tubs were incorporated into the redesigns of the stroke, now called the "micro-stroke." The advantages of this design are given in another section of this report. These devices were interconnected via the crossover tubs and a special mask to form the required contacts to form a binary counter. Performance was excellent with tubs used for carrying signal and power, proving the technique of interconnection under both conditions.

These results and accomplishments of the interconnection matrix with two planes, brought the decision to discontinue the ground return through the substrate effort. This will eliminate the need for the epitaxial growth for production units.

NON-LINEAR LOAD SWITCH DESIGN

In the past quarter, more detailed analysis and first attempts at fabrication have been performed on the non-linear load switch for magnetic power supply synchronizer. An approximate schematic of the circuit to be realized is shown in Figure 5. Study of the device requirements yielded a complex structure that would be difficult to realize even in an optimized structure such as the one shown in Figure 6. For reasons of improved reliability and ease of fabrication, it was decided to construct the output drivers in two sections: the NPN portion and the PNP. This will allow optimization of characteristics of both types of devices and increase the safety of the design thus increasing reliability.

Shown in Figure 7 is a cross section of the structure be used for fabrication of the NPN portion of the output switch. Several test wafers have been processed part way through the process. Checks made on these show that the isolation regions did not proceed as rapidly as expected, so adjustments in the process have been made to obtain the desired result. Subsequent runs are now in process.

The fabrication of the PNP portion will be started follow-in the confirmation of techniques in the NPN portion. The proposed structure is shown in Figure 8.

SCHEMATIC OF NON-LINEAR LOAD SWITCH

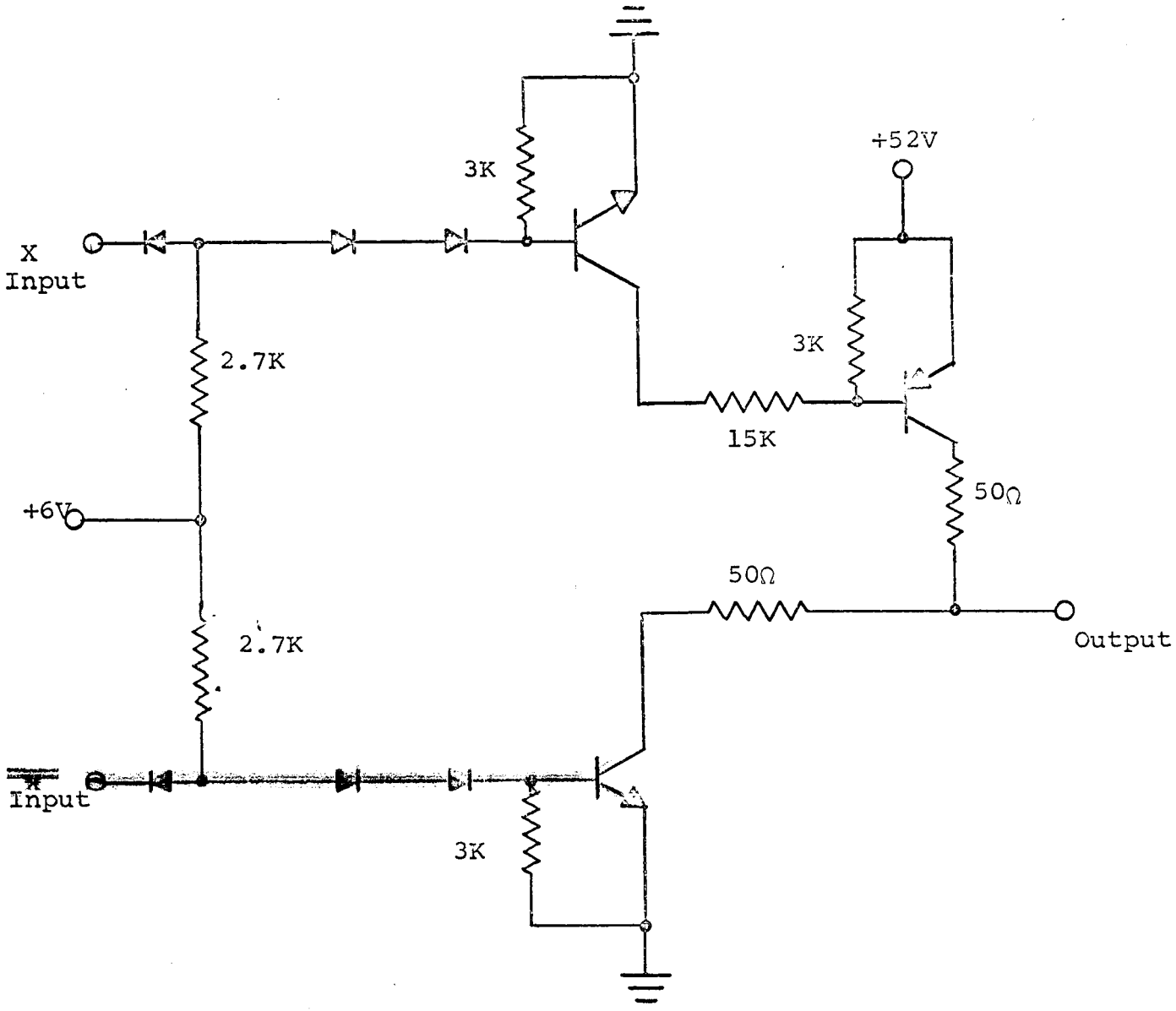

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Figure 5

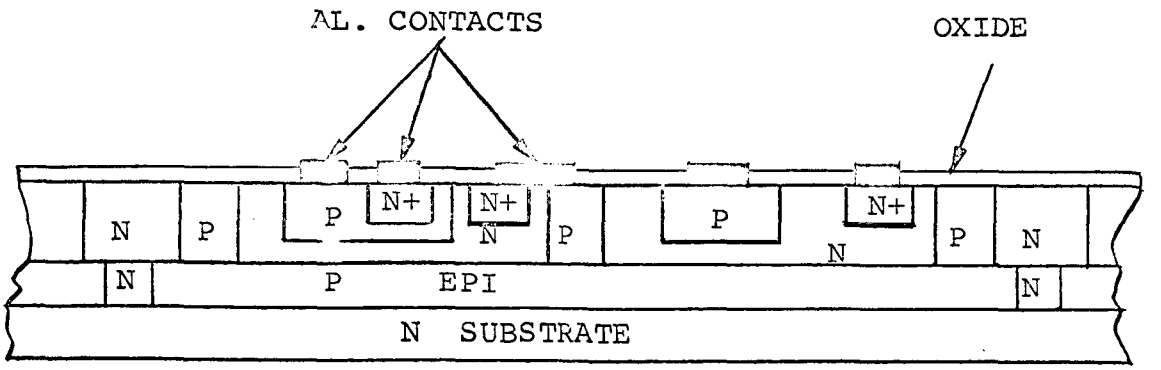

Figure 6

A PROPOSED UNIFIED OUTPUT SWITCH DESIGN

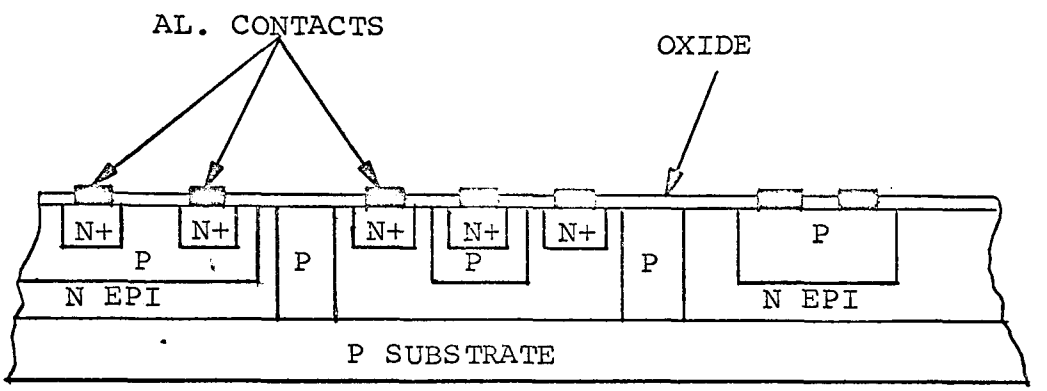

Figure 7

HIGH VOLTAGE STROKE

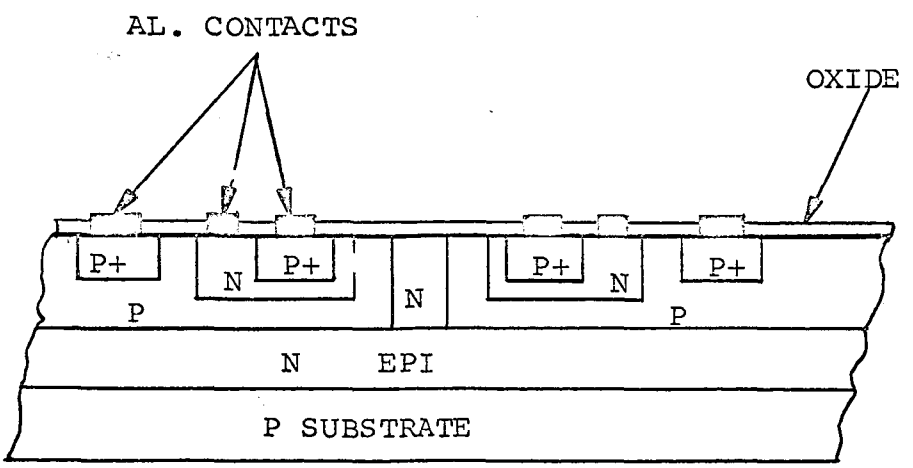

Figure 8

PNP OUTPUT SWITCH LOAD

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PACKAGING DESIGN

Package During this reporting period, our packaging concepts have changed quite drastically. Two events were major factors in this change. The first was a meeting with representatives of JPL during which mounting concepts for the package were discussed and solutions worked out which would permit acceptable mounting methods, and at the same time, have certain advantages from the semi-conductor device point of view. This concept basically is to mount the package in an inverted position with the leads emmerging from the top and fanned out to make contact to a printed circuit board. A preliminary sketch of this concept which involes the silicon chip mounted in the portion of the package which is normally considered to be the cap is shown in Figure 9.

The second important event during this reporting period was the bringing of the new Westinghouse micro-stroke into production so this unit could be used to form the logic for this project. The micro-stroke size is approximately one fourth that of the old stroke and thus permits reducing the overall size of the sub-system, and, therefore, changes many of the packaging concepts. The present projected size for the entire sub-system is .275" x .275" and this permits mounting it in a TO-8 size header. An artist's sketch of this concept is shown in Figure 10.

Lead Weld and Die Attach The original concepts for lead welding with multiple wires of very short length has been retained. Die attach tests using tungsten substrates for thermal matching are being made. However, it is hoped that the reduced size of the chip required to do the sub-system will permit conventional die attach methods to be used and tests will be made in the near future to determine the feasibility of using standard die attach methods.

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TOTAL HEIGHT OF PACKAGE : .250 MAX.

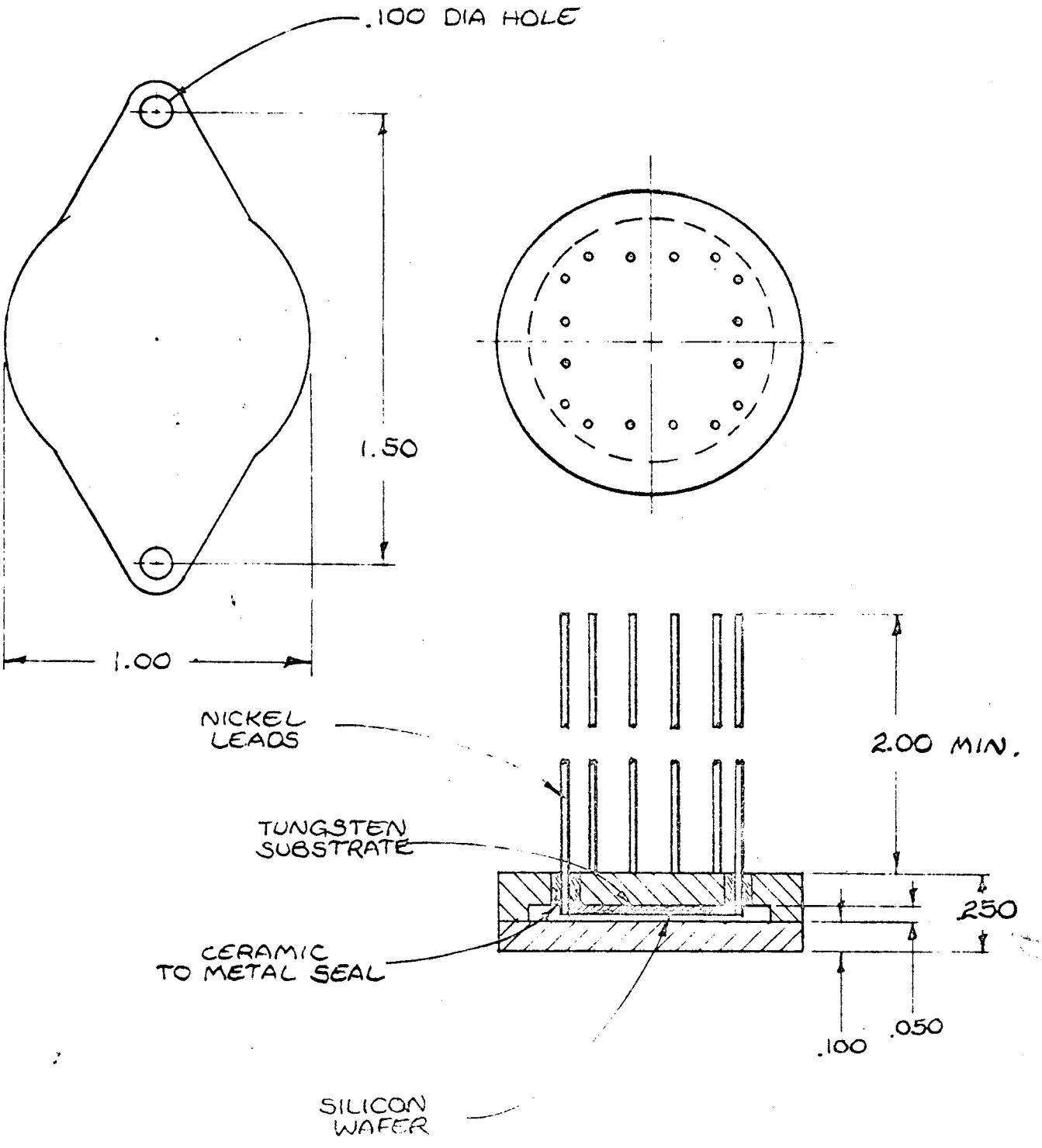

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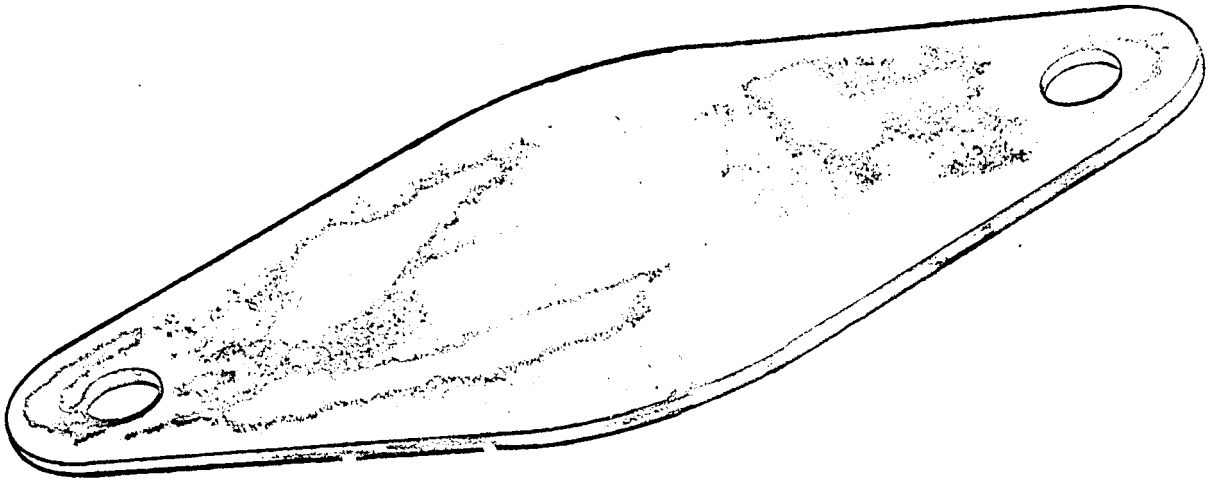
Figure 9

HEADER FOR MICROSTROKES



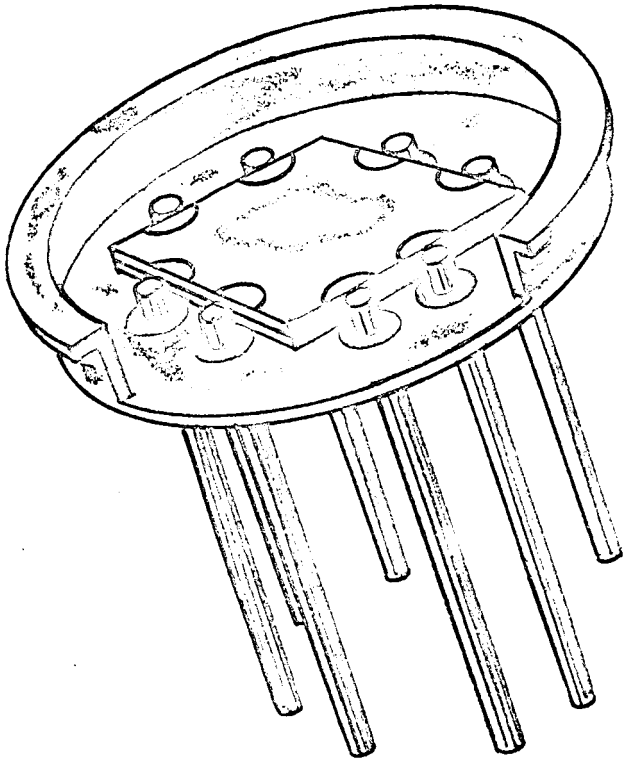


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Figure 10

PARTIAL SYSTEM FABRICATION

With the completion of the binary, in addition to the advantages of proving our interconnect method design, this particular combination of dual NAND gates constitutes the first step in the Partial System Fabrication. The operation of these units has been very satisfactory. The speed attained is far in excess of that required for this project. However, this does not hurt the project in any way and the extra speed is a function of the small geometry used, therefore, there is a definite gain in mounting and in size for the project from this added speed. Typically these binary counters run at about 4 1/2 megacycles as an upper speed limit, therefore, they have no problems at the 38.4 KC requirement of this project. No multi-stage counters have been made by this method, because this pattern does not automatically connect for that; however, single stage counters have been made with yields as high as 66% across a wafer.

A yield improvement program has been in progress during these three months in order to bring yields into line with the requirements for the large number of dual strokes interconnected into a single pattern. These yield improvements

have been brought about by new deposition techniques and have brought total yields from something in the order of 20% at die sort to levels in the 50 and 60% regions at die sort. The changed processes to accomplish this are now completed and are in use on all manufacturing runs. Additional yield improvement, however, is expected as controls are tightened. These controls are constantly being observed, reviewed, and tightened, and during this next three months period, we expect addtional significant yield improvements to take place.

OVERALL SYSTEM FABRICATION

Overall system fabrication has not yet started.